REMARKS

Claims 1 through 4 are currently pending in the application. Applicants have amended claims 1-4, and respectfully request reconsideration of the application as amended herein.

The present claims 1-4 were previously presented in a copending patent application 09/776, 387 as claims 1, 2, 6 and 7, respectively. In the interest of expediting prosecution, Applicants herein respond to the previous rejections in view of the previously cited references. Applicants have renumbered (e.g., previous claim 1 is now current claim 1, previous claim 2 is now current claim 2, previous claim 6 is now current claim 3 and previous claim 7 is now current claim 4) the previously rejected claims in the rejections/responses below to correspond to the current claim numbering in the presently presented continuation application.

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 4,737,830 to Patel et al.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Patel et al. (U.S. Patent No. 4,737,830). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Patel reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 1 because the Patel reference does not describe, either expressly or inherently, the identical invention in as complete detail as are contained in the claim. More specifically, Applicants submit that the Patel reference does not describe, either expressly or inherently, the elements of the claimed inventions of presently amended independent claim 1 calling for

> A semiconductor device system . . . comprising:
> a **carrier substrate**; and
> a semiconductor device . . . coupled to the carrier substrate and including:
> a semiconductor substrate having active circuit devices thereon; and

> an **on-chip capacitor** including at least a portion thereof being **formed** in an active area of the semiconductor substrate **underlying at least two bus signals of the active circuit devices**, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to provide filtering capacitance for the semiconductor device. (Emphasis added.)

While the Office Action-cited "carrier substrate 28" of Patel is actually a semiconductor substrate, Patel does not appear to teach of **"an** on-chip capacitor . . . underlying **at least two** bus signals of the active devices . . ." as claimed by Applicants. In Patel, one or more capacitors appear to be placed along the length of an individual bus signal. Therefore, Applicants respectfully request that the rejection be withdrawn.

Anticipation Rejection Based on Patent No. JP 61-269317 to Hoashi

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hoashi (Patent No. JP 61-269317). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Hoashi reference does not an cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 1 because the Hoashi reference does not describe, either expressly or inherently, the identical invention in as complete detail as are contained in the claim. The Hoashi reference is drawn to an **off**-chip capacitor formed off of the substrate between "the back surface of the semiconductor chip and the lead frame". It appears that the Examiner has, perhaps, misinterpreted the teachings of Hoashi. For example, Hoashi fails to teach an "on-chip" capacitor, or, stated another way, a capacitor formed or otherwise located in a semiconductor die. Instead, the Hoashi capacitor is formed by "providing a dielectric material or empty layer between the back surface of a semiconductor chip and the lead frame." (Hoashi). Furthermore, contrary to the Examiner's

assertions, Applicants can find no teachings in Hoashi of an on-chip capacitor including at least a portion thereof being formed in an active area of the semiconductor substrate underlying at least two bus signals of the active circuit devices, as claimed by Applicants.

Accordingly, it is respectfully submitted that claim 1 is not anticipated by Hoashi, as each and every element of the amended independent claim is not found in the reference. Therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,737,830 to Patel et al.

Claim 2 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Patel et al. (U.S. Patent No. 4,737,830). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Patel reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 2 because the Patel reference does not describe, either expressly or inherently, the identical invention in as complete detail as are contained in the claim. More specifically, Applicants submit that the Patel reference does not describe, either expressly or inherently, the elements of the claimed inventions of presently amended independent claim 2 calling for

> A semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising:
> a semiconductor substrate;
> active circuit devices on the semiconductor substrate; and
> **a capacitor** having at least a portion thereof **formed** in an active area of the semiconductor substrate **underlying at least two bus signals of the active circuit devices**, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device when the semiconductor device is operably connected to the carrier substrate. (Emphasis added.)

Patel does not appear to teach of "**a capacitor** . . . underlying **at least two bus signals of the active circuit devices** . . ." as claimed by Applicants. In Patel, one or more capacitors appear to be placed along the length of an individual bus signal. Therefore, Applicants respectfully request that the rejection be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,737,830 to Patel et al.

Claim 3 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Patel et al. (U.S. Patent No. 4,737,830). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Patel reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 3 because the Patel reference does not describe, either expressly or inherently, the identical invention in as complete detail as are contained in the claim. More specifically, Applicants submit that the Patel reference does not describe, either expressly or inherently, the elements of the claimed inventions of presently amended independent claim 3 calling for

> A semiconductor die assembly configured for connection to external circuitry, the semiconductor die assembly comprising:
> a carrier substrate configured for providing power and ground for at least one semiconductor die operably connected thereto; and
> at least one semiconductor die operably connected to the carrier substrate and including:
> a semiconductor substrate having active circuit elements formed on an active area thereof; and
> **at least one capacitor** on the semiconductor substrate, at least a portion of the at least one capacitor being **formed** on the active area **underlying at least two bus signals of the active circuit elements**, the at least one capacitor being operably coupled to the active circuit elements to provide filtering capacitance for the at least one semiconductor die. (Emphasis added.)

Patel does not appear to teach of "**at least one capacitor** . . . underlying **at least two bus signals of the active circuit elements** . . ." as claimed by Applicants. In Patel, one or more capacitors appear to be placed along the length of an individual bus signal. Therefore, Applicants respectfully request that the rejection be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,737,830 to Patel et al.

Claim 4 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Patel et al. (U.S. Patent No. 4,737,830). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Patel reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of amended independent claim 4 because the Patel reference does not describe, either expressly or inherently, the identical invention in as complete detail as are contained in the claim. More specifically, Applicants submit that the Patel reference does not describe, either expressly or inherently, the elements of the claimed inventions of presently amended independent claim 4 calling for

> A semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising:
> a semiconductor substrate having active circuit elements formed on an active area thereof;
> **at least one capacitor** on the semiconductor substrate, at least a portion of the at least one capacitor being **formed** on the active area **underlying at least two bus signals of the active circuit elements**, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefor when the semiconductor device is operably connected to power and ground of the carrier substrate. (Emphasis added.)

Patel does not appear to teach of "**at least one capacitor** . . . underlying **at least two bus**

signals of the active circuit elements . . ." as claimed by Applicants. In Patel, one or more capacitors appear to be placed along the length of an individual bus signal. Therefore, Applicants respectfully request that the rejection be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al. in view of Research Disclosure (RD 254042)

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Frankeny et al. (U.S. Patent No. 4,903,113) in view of Research Disclosure (RD 254042). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 1 is improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Applicants submit that any proposed combination of the Frankeny reference and the RD 254042 reference do not teach or suggest the claim limitations calling for

> A semiconductor device system . . . comprising:
> a **carrier substrate**; and
> a semiconductor device . . . coupled to the carrier substrate and including:
> a semiconductor substrate having active circuit devices thereon; and
> an **on-chip capacitor** including at least a portion thereof being **formed** in an active area of the semiconductor substrate **underlying at least two bus signals of the active circuit devices**, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to

> provide filtering capacitance for the semiconductor device. (Emphasis added.)

Upon a close reading of Frankeny, it is determined that Frankeny teaches or suggests a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does not teach or suggest an "on-chip" capacitor but rather discloses a separate and discrete "in-package" capacitor.

Regarding the cited Research Disclosure RD 254042, the Office Action states that RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor." (Office Action p. 5). Applicants respectfully acknowledge the gratuitous statement from the cited reference that "capacitors on-chip involve[] virtually zero series inductance", however, the cited reference does not teach or suggest how such capacitors are formed or the composition of such structures.

Therefore, since neither Frankey nor RD 254042, either individually or in any proper combination, teach each and every element of Applicants' invention as claimed, the rejection is improper and should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 4,656,605 to Clayton in view of Research Disclosure (RD 254042)

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Clayton (U.S. Patent No. 4,656,605) in view of Research Disclosure (RD 254042). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable

> expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 1 is improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Applicants submit that any proposed combination of the Clayton reference and the RD 254042 reference do not teach or suggest the claim limitations calling for

> A semiconductor device system . . . comprising:
> a **carrier substrate**; and
> a semiconductor device . . . coupled to the carrier substrate and including:
> a semiconductor substrate having active circuit devices thereon; and
> an **on-chip capacitor** including at least a portion thereof being **formed** in an active area of the semiconductor substrate **underlying at least two bus signals of the active circuit devices**, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to provide filtering capacitance for the semiconductor device. (Emphasis added.)

Clayton teaches or suggests that "[a]lso ***mounted on*** the substrate of module 30 are small ceramic decoupling capacitors 33-40, having a value between 0.1 and 0.22 ufd, and connected between each of memory chips 10-18 to suppress transient voltage spikes." (Col. 2, lines 57-61; Emphasis added.) Clayton does <u>not</u> teach or suggest an "on-chip" capacitor but rather "ceramic" capacitors ***"mounted on"*** the substrate.

Regarding the cited Research Disclosure RD 254042, the Office Action states that RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor." (Office Action p. 5). Applicants respectfully acknowledge the gratuitous statement from the cited reference that "capacitors on-chip involve[] virtually zero series inductance", however, the cited reference does not teach or suggest <u>how</u> such capacitors are formed or the composition of such structures.

Therefore, since neither Clayton nor RD 254042, either individually or in any proper combination, teach each and every element of Applicants' invention as claimed, the rejection is

improper and should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 4,656,605 to Clayton in view of Research Disclosure (RD 254042)

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Clayton (U.S. Patent No. 4,656,605) in view of Research Disclosure (RD 254042). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 2 is improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Applicants submit that any proposed combination of the Clayton reference and the RD 254042 reference do not teach or suggest the claim limitations calling for

> A semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising:
> a semiconductor substrate;
> active circuit devices on the semiconductor substrate; and
> **a capacitor** having at least a portion thereof **formed** in an active area of the semiconductor substrate **underlying at least two bus signals of the active circuit devices**, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device when the semiconductor device is operably connected to the carrier substrate. (Emphasis added.)

Clayton teaches or suggests that "[a]lso ***mounted on*** the substrate of module 30 are small ceramic decoupling capacitors 33-40, having a value between 0.1 and 0.22 ufd, and connected between each of memory chips 10-18 to suppress transient voltage spikes." (Col. 2, lines 57-61; Emphasis added.) Clayton does not teach or suggest an "on-chip" capacitor but rather "ceramic" capacitors ***"mounted on"*** the substrate.

Regarding the cited Research Disclosure RD 254042, the Office Action states that RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor." (Office Action p. 5). Applicants respectfully acknowledge the gratuitous statement from the cited reference that "capacitors on-chip involve[] virtually zero series inductance", however, the cited reference does not teach or suggest how such capacitors are formed or the composition of such structures.

Therefore, since neither Clayton nor RD 254042, either individually or in any proper combination, teach each and every element of Applicants' invention as claimed, the rejection is improper and should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al. in view of Research Disclosure (RD 254042)

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Frankeny et al. (U.S. Patent No. 4,903,113) in view of Research Disclosure (RD 254042). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 3 is improper because the

elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Applicants submit that any proposed combination of the Frankeny reference and the RD 254042 reference do not teach or suggest the claim limitations calling for

> A semiconductor die assembly configured for connection to external circuitry, the semiconductor die assembly comprising:
> a carrier substrate configured for providing power and ground for at least one semiconductor die operably connected thereto; and
> at least one semiconductor die operably connected to the carrier substrate and including:
> a semiconductor substrate having active circuit elements formed on an active area thereof; and
> **at least one capacitor** on the semiconductor substrate, at least a portion of the at least one capacitor being **formed** on the active area **underlying at least two bus signals of the active circuit elements**, the at least one capacitor being operably coupled to the active circuit elements to provide filtering capacitance for the at least one semiconductor die. (Emphasis added.)

Upon a close reading of Frankeny, it is determined that Frankeny teaches or suggests a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does not teach or suggest an "on-chip" capacitor but rather discloses a separate and discrete "in-package" capacitor.

Regarding the cited Research Disclosure RD 254042, the Office Action states that RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor." (Office Action p. 5). Applicants respectfully acknowledge the gratuitous statement from the cited reference that "capacitors on-chip involve[] virtually zero series inductance", however, the cited reference does not teach or suggest how such capacitors are formed or the composition of such structures.

Therefore, since neither Frankey nor RD 254042, either individually or in any proper combination, teach each and every element of Applicants' invention as claimed, the rejection is improper and should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al. in view of Research Disclosure (RD 254042)

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Frankeny et al. (U.S. Patent No. 4,903,113) in view of Research Disclosure (RD 254042). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claim 4 is improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claim limitations.

Applicants submit that any proposed combination of the Frankeny reference and the RD 254042 reference do not teach or suggest the claim limitations calling for

> A semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising:
> a semiconductor substrate having active circuit elements formed on an active area thereof;
> **at least one capacitor** on the semiconductor substrate, at least a portion of the at least one capacitor being **formed** on the active area **underlying at least two bus signals of the active circuit elements**, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefor when the semiconductor device is operably connected to power and ground of the carrier substrate. (Emphasis added.)

Upon a close reading of Frankeny, it is determined that Frankeny teaches or suggests a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional

technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does not teach or suggest an "on-chip" capacitor but rather discloses a separate and discrete "in-package" capacitor.

Regarding the cited Research Disclosure RD 254042, the Office Action states that RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor." (Office Action p. 5). Applicants respectfully acknowledge the gratuitous statement from the cited reference that "capacitors on-chip involve[] virtually zero series inductance", however, the cited reference does not teach or suggest how such capacitors are formed or the composition of such structures.

Therefore, since neither Frankey nor RD 254042, either individually or in any proper combination, teach each and every element of Applicants' invention as claimed, the rejection is improper and should be withdrawn.

ENTRY OF AMENDMENTS

The amendments to claims 1-4 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1-4 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Kevin K. Johanson
Registration No. 38,506
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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